

### REMARKS

Claims 1-4, 6, 8-12, 14, 16-18, and 20-24 are pending in the Application. Claims 1, 9, and 17 are independent claims. Claims 1, 9, and 17 have been amended. Claims 5, 7, 13, 15, and 19 have been canceled.

#### *Claim Rejections - 35 USC § 103(a)*

The Patent Office rejected Claims 1-4, 8-12, 16-17 and 24 under 35 U.S.C. § 103(a) as being unpatentable over Voogel et al. (U.S. Patent No. 6,362,651) (“Voogel”) in view of Hongo et al. (U.S. Publication No. 2003/0143971) (“Hongo”) further in view of Glenn et al. (U.S. Patent No. 6,962,829) (“Glenn”). The Patent Office also rejected Claims 6 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Voogel in view of Hongo further in view of Glenn and Mastro et al. (U.S. Publication No. 2002/0091977) (“Mastro”). The Patent Office also rejected Claims 18 and 20-23 under 35 U.S.C. § 103(a) as being unpatentable over Voogel in view of Hongo further in view of Glenn and Lee et al. (U.S. Patent No. 6,222,212) (“Lee”).

Applicant respectfully traverses the rejections. “The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness.” MPEP § 2142. In order to establish a prima facie case, the examiner must ascertain the differences between the claim and the prior art. MPEP § 2141. “All words in a claim must be considered in judging the patentability of that claim against the prior art.” MPEP § 2143.03, citing *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). “If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious.” MPEP § 2143.03, citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicant respectfully submits Claims 1-4, 6, 8-12, 14, 16-18, and 20-24 include elements that are not disclosed by the available prior art. For example, Claim 1 recites: “A method for providing field programmable platform array units...said plurality of platform array units

having...interconnect between said plurality of platform array units being pre-routed on chip...wherein said interconnect between said plurality of platform array units is at least one of direct, via bus-bars, and via network on chip.” Voogle, Hongo, and Glenn, alone or in combination, do not disclose the above limitations. The Patent Office cites to Voogle for disclosing the pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip, stating that “said plurality of platform array units having...interconnect 610 between said plurality of platform array units 450(1) & 450(2) being pre-routed on chip (Fig. 6)” (August 11, 2009 Office Action, p. 3) (“Office Action”). However, Applicant respectfully disagrees with this interpretation of Voogle. The accompanying text to the cited portion of Voogle recites: “Signal transmission in IOB-on-IOB device-linking conductor 610 passes through a pass gate 620, which is controlled by configuration memory cell M20” (Col. 8, ll. 40-43.). Disclosing a device-linking conductor passes through a pass gate, which is controlled by a configuration memory cell is not equivalent to disclosing a method for providing field programmable platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip.**

The disclosure of Hongo does not cure the defects of Voogel. The Patent Office cites to Hongo for disclosing a DSP platform “chip including at least one core and at least one processor...encapsulation 550 of lower metal layers...preserved by a standard die seal” (Office Action, p. 3). A DSP platform chip including at least one core and at least one processor, the chip lower metal layers preserved by a standard die seal, is not equivalent to a method for providing field programmable platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip.** Neither Hongo nor Voogel disclose a pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip. Hongo and Voogel, alone or in combination, do not disclose a method for providing field

programmable platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip.**

The disclosure of Glenn does not cure the defects of Voogel and Hongo. Glenn is cited for disclosing the chip lower metal layers are the lower copper metal layers (Office Action, p. 4). The chip lower metal layers being the lower copper metal layers is not equivalent to a method for providing field programmable platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip.** Neither Glenn nor Hongo and Voogel disclose a pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip. Glenn, Hongo, and Voogel, alone or in combination, do not disclose a method for providing field programmable platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip.** Claim 1 is believed allowable for at least the above reasons.

Claims 2-4 and 8 depend upon Claim 1 either directly or indirectly and are allowable under *In re Fine* based on their dependence upon allowable base claims.

Similarly, Claim 9 recites: “A system for providing field programmable platform array units...said plurality of platform array units having...interconnect between said plurality of platform array units being pre-routed on chip...wherein said pre-routed interconnect is at least two of direct, via bus-bars, and via network on chip.” Voogel, Hongo, and Glenn, alone or in combination, do not disclose the above limitations. The Patent Office cites to Voogel for disclosing the pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip, stating that “said plurality of platform array units having...interconnect 610 between said plurality of platform array units 450(1) & 450(2) being pre-routed on chip (Fig. 6)” (Office Action, p. 3).

However, Applicant respectfully disagrees with this interpretation of Voogle. The accompanying text to the cited portion of Voogle recites: “Signal transmission in IOB-on-IOB device-linking conductor 610 passes through a pass gate 620, which is controlled by configuration memory cell M20” (Col. 8, ll. 40-43.). Disclosing a device-linking conductor passes through a pass gate, which is controlled by a configuration memory cell is not equivalent to disclosing a system for providing field programmable platform array units, said plurality of platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least two of direct, via bus-bars, and via network on chip.**

The disclosure of Hongo does not cure the defects of Voogel. The Patent Office cites to Hongo for disclosing a DSP platform “chip including at least one core and at least one processor...encapsulation 550 of lower metal layers...preserved by a standard die seal” (Office Action, p. 3). A DSP platform chip including at least one core and at least one processor, the chip lower metal layers preserved by a standard die seal, is not equivalent to a system for providing field programmable platform array units, said plurality of platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least two of direct, via bus-bars, and via network on chip.** Neither Hongo nor Voogel disclose a pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip. Hongo and Voogel, alone or in combination, do not disclose a system for providing field programmable platform array units, said plurality of platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least two of direct, via bus-bars, and via network on chip.**

The disclosure of Glenn does not cure the defects of Voogel and Hongo. Glenn is cited for disclosing the chip lower metal layers are the lower copper metal layers (Office Action, p. 4). The chip lower metal layers being the lower copper metal layers is not equivalent to a system for providing field

programmable platform array units, said plurality of platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least two of direct, via bus-bars, and via network on chip.** Neither Glenn nor Hongo and Voogel disclose a pre-routed interconnect is at least two of direct, via bus-bars, and via network on chip. Glenn, Hongo, and Voogel, alone or in combination, do not disclose a system for providing field programmable platform array units, said plurality of platform array units having interconnect between said plurality of platform array units being pre-routed on chip, **wherein said pre-routed interconnect is at least two of direct, via bus-bars, and via network on chip.** Claim 9 is believed allowable for at least the above reasons.

Claims 10-12 and 16 depend upon Claim 9 either directly or indirectly and are allowable under *In re Fine* based on their dependence upon allowable base claims.

Similarly, Claim 17 recites: “a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer...wherein interconnect between said plurality of platform array units being pre-routed...wherein said pre-routed interconnect is at least one of via bus-bars and via network on chip.” Voogel, Hongo, and Glenn, alone or in combination, do not disclose the above limitations. The Patent Office cites to Voogel for disclosing the pre-routed interconnect is at least one of direct, via bus-bars, and via network on chip, stating that “said plurality of platform array units having...interconnect 610 between said plurality of platform array units 450(1) & 450(2) being pre-routed on chip (Fig. 6)” (Office Action, p. 3). However, Applicant respectfully disagrees with this interpretation of Voogel. The accompanying text to the cited portion of Voogel recites: “Signal transmission in IOB-on-IOB device-linking conductor 610 passes through a pass gate 620, which is controlled by configuration memory cell M20” (Col. 8, ll. 40-43.). Disclosing a device-linking conductor passes through a pass gate, which is

controlled by a configuration memory cell is not equivalent to disclosing a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, wherein interconnect between said plurality of platform array units being pre-routed, **wherein said pre-routed interconnect is at least one of via bus-bars and via network on chip.**

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The disclosure of Glenn does not cure the defects of Voogel and Hongo. Glenn is cited for disclosing the chip lower metal layers are the lower copper metal layers (Office Action, p. 4). The chip lower metal layers being the lower copper metal layers is not equivalent to a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, wherein interconnect between said plurality of platform array units being pre-routed, **wherein said pre-routed interconnect**

**is at least one of via bus-bars and via network on chip.** Neither Glenn nor Hongo and Voogel disclose a pre-routed interconnect is at least one of via bus-bars and via network on chip. Glenn, Hongo, and Voogel, alone or in combination, do not disclose a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, wherein interconnect between said plurality of platform array units being pre-routed, **wherein said pre-routed interconnect is at least one of via bus-bars and via network on chip.** Claim 17 is believed allowable for at least the above reasons.

Claim 24 depends upon Claim 17 either directly or indirectly and is allowable under *In re Fine* based on their dependence upon allowable base claims.

The Patent Office rejected Claims 6 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Voogel in view of Hongo further in view of Glenn and Mastro. Applicant respectfully traverses. Claim 6 depends from Claim 1, which is allowable for the reasons stated above, and is believed allowable under *In re Fine* based on its dependence upon an allowable base claim. Claim 14 depends from Claim 9, which is allowable for the reasons stated above, and is thus believed allowable under *In re Fine* due to its dependence upon an allowable base claim.

The Patent Office rejected Claims 18 and 20-23 under 35 U.S.C. § 103(a) as being unpatentable over Voogel in view of Hongo further in view of Glenn and Lee. Applicant respectfully traverses. Claims 18 and 20-23 depend from Claim 17, which is allowable for the reasons stated above, and are believed allowable under *In re Fine* due to their dependence on an allowable base claim.

For at least the above reasons, allowance of Claims 1-4, 6, 8-12, 14, 16-18, and 20-24 is respectfully requested.

**CONCLUSION**

In light of the forgoing, reconsideration and allowance of the claims is earnestly solicited.

Respectfully submitted,  
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